Dr. UDAY PANWAR
S/O Mr. M.S. PANWAR
140, Aradhana Nagar, BHOPAL (M.P)
E-mail: panwaruday1@gmail.com , uday_panwar@iiitvadodara.ac.in
Mobile No: 9826752267

Career Objective:

I am willing to work in a challenging environment, to put in my inherent skills and abilities for effective utilization and productivity of the organization.

Experience: 13 Years **3** Month **22** Days **(Post PhD**. Exp**: 10 Y 8 M)**

Current Employer: -

Assistant Professor in Department of Electronics and Communication Engg. at **Indian Institute of Information Technology, Vadodara International Campus Diu (IIITV-ICD)** – 17th Feb 2026 to till date.

Previous Experience-

1) Assistant Professor School of Technology, Management & Engineering - Faculty of Electronics & Tele Communication (STME-EXTC Dept.) **Narsee Monjee Institute of Management Studies (NMIMS) Hyderabad**- 24th July 2025 to 10th Feb 2026.
   - Entrepreneurship Cell Coordinator
   - Mentor: Robotics Club (Vinyasa)
   - Member of IEEE - 101792888 (IEEE Region: R10 -Asia and Pacific) Till Dec 2027

2) **Professor & HoD of** Electronics & Communication Engineering Department at **Sagar Institute of Research & Technology (SIRT-NBA, NAAC accredited),** Bhopal (M.P.) from **09-02-2015** to **16-07-2025**.

Administration Responsibilities

- MSME HI & SKYNEST **Incubation Center Coordinator** at SGI.
- **Group Convener** of **Entrepreneur Development Cell** of SIRT, Bhopal since 20th Sept, 2019
- **Start-Up Coordinator &Member of** Institute Innovation Council (IIC) of SIRT, Bhopal since 05th Aug, 2019
- **PG Institute Coordinator** since 21st Dec 2021.
- **Co- HoD** in ECE department since 19th January 2017 to 27th August 2024.
- **MTech Coordinator** in ECE department since 01st Sept 2019.
- **NBA Core Team Member** at SIRT on 8th June 2020.
- **Coordinator** of **Consultancy** Task group EC dept. of SIRT, Bhopal from 20th Sept, 2019 to 1st, Dec 2020.
- **Co-Convener** in Library Task Group Since 9th April 2016 to 01st July, 2018

3) **Maulana Azad National Institute of Technology (M.A.N.I.T) BHOPAL** as an Assistant Professor (Contract) from 05-07-2013 to 31-12-2013.
4) **Maulana Azad National Institute of Technology (M.A.N.I.T) BHOPAL** as an Assistant Professor (Contract) from 15-07-2011 to 31-03-2012

 # Worked under SMDP Project at Maulana Azad National Institute of Technology (MANIT) Bhopal with Cadence Virtuoso, HSpice Synopsis, Tanner Mentor Graphics, Xilinx ISE.

5) **Maulana Azad National Institute of Technology (M.A.N.I.T)** as a contract Lecturer from 29-07-2010 to 31-12-2010.
6) **Swami Vivekananda College of Engineering (S.V.C.E) INDORE** as a Lecturer from 06-08-2009 to 06-03-2010.

Academic and Professional Qualifications:

EXAM/DEGREE	BOARD/ UNIVERSITY	YEAR OF PASSING	DIVISION	Percentage (%)
Ph.D. (**VLSI Design**)	Maulana Azad National Institute of Technology, Bhopal	9th July 2015	Awarded	Course work = 9.12
M.E (**Digital Comm. Engg**.)	Devi Ahilya VishwaVidyalaya, Indore	2009	First &Distinction	76.93
B.E.(**Electronics & Communication Engg**)	Rajiv Gandhi Technical University (R.G.P.V) Bhopal	2006	First(Hon's)	75.56
12th	Dayanand Arya Vedic Higher Secondary School	2002	First	72.40
10th	Dayanand Arya Vedic Higher Secondary School	2000	First &Distinction	82.00

Ph.D. Title: GATE REPLACEMENT TECHNIQUE FOR REDUCING WORST LEAKAGE CURRENT IN DSM CIRCUITS
Supervisor: **Dr Kavita Khare** , Professor , ECE Dept.
Institute**: MAULANA AZAD NATIONAL INSTITUTE OF TECHNOLOGY, BHOPAL**
Date of Defense Viva: **9th July, 2015** Date of Award: **16th April, 2016**

Skills:

EDA Tools Known	Cadence (VIRTUOSO, PSPICE),Synopsys-(HSPICE),Tanner, Xilinx ISE, EDA Win XP, Multisim, LTspice
Hardware Description Languages	VHDL(Very High Speed Integrated Circuits Hardware Description Language), Verilog
Computer Languages	Python Programming(NPTEL certified),

Industrial Trainings:

Minor Training: B.S.N.L (Bhopal) (from 18/07/2005 to 30/07/2005)
Major Training: Doordarshan Kendra Bhopal (from 20/06/2005 to 16/07/2005)

Patent: # 6 Patents published at Intellectual Property of India

Grant :

1. **International Patent** on Title: **PCML – Movable Satellite: Propagation Impairments for Movable Satellite Communication Links at the Microwave Frequency in Defined Location**. Patent No. #2020102544 Application filing date: 4th, Nov 2020

Published:

2. Title: **IPCPC-VLSI-CIRCUIT: Intelligence Process of computing dual Conductor Parasitic Advanced Capacitances for VLSI Circuits**.
   Patent No. #202041006276, Application Publication date: 21st Feb 2020.
3. Title: **ITMD Device: Intelligent Technology to Maximize Display area of a Mobile Devices.**
   Patent No. #202011009101, Application Publication date: 20th March 2020
4. Title: **PD MASS STORAGE LOCKING: PEN DRIVE MASS STORAGE LOCKING**.
   Patent No. #202041015048, Application Publication date: 22nd May 2020
5. Title: **MELT-SUBSTRATE RGB-COLOR 3D WRITING PEN**
   Patent No. #202011015754, Application Publication date: 26th June 2020
6. Title: **CNDMP-User Tracking & Current Location Notification Using IoT Based Deep Machine Learning Programming**
   Patent No. #202021014117, Application Publication date: 29th June 2021

Copyright: - (i) Experiential Learning with Circuit Analysis
Registration Number L-126795/2023, at 5 Aug 2023
(ii) Raspberry Pi Based Vehicle Ignition System Activation by Face Detection,
Registration Number L-131341/2023 at 2 Aug 2023
(iii) Presentation On (A) IPR Basics and (B) Patent Filing Procedure in India,
Registration Number no.: L-106750/2021 on 23 Aug 2021.

UG Projects Under Taken:

- Major Project- "Tele Metering"
- Minor Project- "Telephone Link Monitor"

Subjects of Interest:

- VLSI Design,
- Network Analysis,
- Analog and Digital communication,
- Digital electronics,

Publication

My Publication

Book

1) Dr Uday Panwar published a Book, "Adiabatic Logic Circuit Design for Nano Scale Low Power Application, Subtitle: CNTFET based Nano Scale Digital circuit designing for ULSI Application", ISSN no. 978-620-9-21185-0, Published on **2025** Publishing house LAP LAMBERT Academic Publishing. Buy Adiabatic Logic Circuit Design for Nano Scale Low

Power Application Book Online at Low Prices in India | Adiabatic Logic Circuit Design for Nano Scale Low Power Application Reviews & Ratings - Amazon.in

2) Dr Shalini Sahay, Dr. Uday Panwar, "Optimization Analysis of Speech Processing Based Alzheimer's Disease", Lambart Academic Publication, **2025**, link : Buy Optimization Analysis of Speech Processing Based Alzheimer's Disease Book Online at Low Prices in India | Optimization Analysis of Speech Processing Based Alzheimer's Disease Reviews & Ratings - Amazon.in.

Book Chapter (SCOPUS Indexed)

Accepted Publication

1) Uday Panwar, Parul Sharma, Ajay Dadoria "**CNTFET-Based Ternary Arithmetic Circuits: A Novel Approach for Ultra-Low Power and High-Speed Applications**", published a chapter in Book "**Next Generation Electronic Devices, Circuits and Applications** ". CRC Press Taylor & Francis. **2026.**

Published

2) **Uday Panwar** Ajay Dadoria "Variants based Gate Modification (VGM) technique for reducing leakage power and short channel effect in DSM circuits" published a chapter in Book, "**Advance MOS Devices and Its Circuit Applications**". CRC Press **Taylor & Francis. JAN 2024.** https://**doi.org**/10.1201/9781032670270. ISBN 9781032670270. PP. 118-130.
3) **Uday Panwar** Ajay Dadoria, Narendra Garg "Measurement of back-gate biasing for ultra-low-power subthreshold logic in FinFET device", published a chapter in Book, "**Advance MOS Devices and Its Circuit Applications**". CRC Press **Taylor & Francis. JAN 2024.** https://**doi.org**/10.1201/9781032670270. ISBN 9781032670270. PP. 49-55.
4) Komal Tahiliani, **Uday Panwar**, "Transforming healthcare through machine learning and deep learning approaches" published chapter in book **Edge-AI in Healthcare: Trends and future perspective**, CRC Press **Taylor & Francis** Publication, PP 45-60, **July 2023**. EISBN: 9781003244592. https://doi.org/10.1201/9781003244592.
5) **Uday Panwar**, Kavita Khare, "Leakage Reduction by Integrating IVC and ALS technique in 65nm CMOS One Bit Adder Circuit", Emerging Research in Computing, Information, Communication and Applications (ERCICA) **Springer**, **31 July 2015**, PP. 469-476.

SCI Journals Published

1) Ajay Kumar Dadoria, Kavita Khare, Tarun kumar Gupta, **Uday Panwar**, "Integrating Flipped Drain and Power Gating Technique for FinFET Logic Circuit", WILEY-IJNM. 31, 5, 1-14, 19th April **2018**. DOI: 10.1002/jnm.2344 (SCI), Online ISSN:1099-1204 IM 1.7

2) Ajay Kumar Dadoria, Kavita Khare, **Uday Panwar**, Anita Jain. "Performance Evaluation of Domino Logic Circuits for wide fan-in gates with FinFET" Microsystem Technologies, Springer, 24, 8, 3341-3348, **2018**. DOI: 10.1007/s00542-017-3691-3 (SCI).
   Print ISSN 0946-7076 ONLINE ISSN 1432-1858 IM 1.581
3) **Uday Panwar**, Kavita Khare; Gate Replacement with PMOS stacking for Leakage reduction in VLSI Circuits; WILEY-IJNM; 29; 4; 565-576; OCT **2015** DOI: 10.1002/jnm.2112(SCI), Online ISSN:1099-1204 IM 1.7

Web of Science/SCOPUS/IEEE Conference Publication

1) Kalyani Tomar, Uday Panwar, Ramji Gupta, "A melanoma skin cancer detection and analysis using dermoscopy image processing", AIP Conference Proceedings, Vol 255, Issue 1, **Dec 2023**.
2) Bhawna Pal, Uday Panwar, "Survey Paper on Massive MIMO System based on Beamforming Technology for mm Wave Communication", Grenze International Journal of Engineering & Technology (GIJET). **2022**, Vol. 8 Issue 1, p491-497.
3) Uday Panwar, Parul Sharma, "Design and Implementation of Ternary Adder for High-Performance Arithmetic Applications by Using CNTFET Material", Materials Today, Elsevier, Volume 63, Pages 773-777, **2022**. DOI: https://doi.org/10.1016/j.matpr.2022.05.316
4) **Uday Panwar**, Anat Shrivastava, "A Novel Technique to improve Performance Evaluation of Domino Logic Circuits in CMOS and FinFET Technology", **IEEE** 2nd International Conference on Data, Engineering and Applications **2020** (IDEA-2k20), 28th -29th, Feb **2020**.
5) Anjali Patware, **Uday Panwar** "A Novel Design CNTFET based Adiabatic Logic Circuit for Low Power Application" in International Journal of Advanced Science & Technology, Elsevier, Vol. 29, No. 7, PP. 5999-6011.**2020**.
6) Namrata Sharma,**Uday Panwar** " A Novel Approach for Analysis CNTFET Based Domino Circuit in Nano Scale Design", in International Journal of Advanced Science & Technology, Elsevier, Vol. 29, No. 7, PP. 5898-5908. **2020.**
7) Ankit Upadhyay, **Uday Panwar**, "High Performance VLSI Architecture for Transpose Form FIR Filter using Integrated Module", **IEEE** Conference on Computer Communication and Informatics (ICCCI -2018), Jan. 04 – 06, **2018**, Coimbatore, INDIA.
8) Mohd Farid Khan, **Uday Panwar**, "A Novel Technique in Adiabatic Logic for Ultra Low Power IN DSM Technology", 2018 International Conference on recent Innovation in

Electrical, Electronics & Communication Engineering (ICRIEECE) on 27th -28th July **2018**, Bhubaneswar, India. Pp 2012-2017, DOI: 10.1109/ICRIEECE44171.2018.9008430.

9) Nidhi Sharma, **Uday Panwar**, Virendra Singh "A Novel Technique of Leakage Power Reduction in 9T SRAM Design in FinFET Technology", **IEEE** Sponsored 6th International Conference-CONFLUENCE – **2016**, 14th -15th Jan 2016, PP.737-743, AMITY university Noida, India.

10) **Uday Panwar** Kavita Khare, "Gate Replacement Technique with Thick Tox to mitigate Leakage with Zero Delay Penalty for DSM CMOS circuit", 2015 **IEEE** conference, International Conference On Industrial Instrumentation, and Control (ICIC 2015), No. 617, May 28-30, **2015**, Pune, India, pp. 836-840.

11) Manikya Vara Prasad Done, **Uday Panwar** Kavita Khare, "an algorithmic approach for leakage current reduction in deep sub-micron CMOS circuits", International Conference On Advances in Electronics, Computers and Communications (ICAECC) October 10–11, **2014**, Bangalore, India, **IEEE** conference, pp. 1-5.

12) **Uday Panwar**, Kavita Khare; Leakage Power Reduction by Adaptive Logic Cell technique in CMOS VLSI Digital circuit design; Mediterrian Journal of Electronics and Communication(MEDJEC); 10; 3; 736-740; Oct **2014 (IET INSPEC)**

National Conference Publication

1) **Uday Panwar**, Ajay Kumar Dadoria, "A Survey On Low Power Adiabatic Logic Circuits In VLSI Circuit Design", International Conference on Advances in Nano materials and Device for Energy & Environment, ICAN-2019 at IIITM Gwalior 27-29 JAN 2019.
2) **Uday Panwar**, Rishabh Singh, "Low Power Nano-Scale Based Adiabatic Logic Circuit Design in VLSI Applications", 6th National Conference on Advanced Materials and Radiation Physics (AMRP-2023) organized by Department of Physics, Sant Longowal Institute of Engineering and Technology, Longowal held during May 18-19, 2023.

Peer Reviewed Journals Published

1) Aamir Siddiqui, Uday Panwar, "Rounding Based Approximate Multiplier (ROBA) For Digital Signal Processing: A Review", International Journal of Innovative Research in Computer and

Communication Engineering, e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 7.488, Volume 8, Issue 9, September **2020**, pp. 3745-3749

2) Harshmani Yadav, **Uday Panwar**, "Design of 8-Bit ALU Design using GDI Techniques with Less Power and Delay', International Journal of Recent Technology and Engineering IJRTE ISSN: 2277-3878 (Online), Volume-8 Issue-4, Nov **2019**. Page No.: 10083-10088.

3) Pratibha Singh Gour, **Uday Panwar**; A Review on Leakage Power on FinFET Technology; CIIT International Journal of Software Engineering and Technology, 10, 8, August **2018**, 161-166. ISSN 0974 – 9632
4) **Uday Panwar**, Himanshu Vishnoi; Diode Switch: A Novel Technique for Mitigation of Leakage Power in DSM Technologies; IJCA, 167; 14,13-19, June **2017** DOI: 10.5120/ijca2017914209
5) Vandana Prajapati,**Uday Panwar**; Power Analysis and Implementation of the 8 - bit Toggle Clock Gated ALU; IJCA;143;8;23-27; June **2016** DOI: 10.5120/ijca2016910202
6) Vandana Prajapati,**Uday Panwar**; Comparative Analysis of Existing Clock Gating ALU; IJSRP;6;5;10-12; MAY **2016**.
7) **Uday Panwar**, Kavita Khare; Backtrack input vector algorithm for leakage reduction in CMOS VLSI Digital Circuit Design; VLSICS; 5; 2; 1-9; Apr **2014** DOI: 10.5121/vlsic.2014.5201.
8) **Uday Panwar**, Kavita Khare; Comparison of Leakage current at Deep Sub Micron technologies in CMOS Digital Circuit; CiiT International Journal of Programmable Device Circuits and Systems; 6; 5; 147-149; May **2014** DOI: PDCS052014003. ISSN 0974 – 9624
9) Manikya Vara Prasad Done, **Uday Panwar**, Kavita Khare; An Algorithm for Leakage Power Reduction through IVC in CMOS VLSI Digital Circuits; IJCA; 94; 7; 24-28; May **2014** DOI: 10.5120/16356-5740.
10) **Uday Panwar**, Kavita Khare; A Combined Approach of IVC and GR for Leakage Power Reduction in CMOS VLSI Digital Circuit; IJCA; 98; 5; 33-37; July **2014**, DOI: 10.5120/17181-7276.
11) **Uday Panwar**, Kavita Khare; Area Leakage Power and delay Optimization By Switched High VTH Logic; IJVES; 5, 1061-1065; June **2014**.
12) **Uday Panwar** Ajay Dadoria; Comparison on Different Domino Logic Design for High Performance and Leakage Tolerant Wide OR Gate; IJERA; 3; 6; Dec **2013**.

Achievements:

Reviewer:
Got opportunity as a reviewer for CBSE Teacher Training Module development on Basic Electronic by CBSE for class 11-12.

Training Program:

1) Successfully Completed one-week Short Term Training Program on **Augmented Reality in Education** at NITTTR Bhopal from 17th- 21st November 2025.

NPTEL course:

1) **Python for Data Science** NPTEL course successfully qualified in **Elite** Category from **Jan-Feb 2024**.

Organized Conferences –

1) Organized 5th National Conference on Recent Trends in IoT, Machine Learning, Artificial Intelligence & It's application (NCRIMA **2024**) on 9th May **2024** at Department of EC, SIRT Bhopal as Program Conference Co-Chair.
2) Organized 2 days "Sixth International Conference On Recent Trends in Engineering, Management Pharmacy and Science – SAGECON2K24" in **SERB Granted** "International Symposium on Modern Technologies of Electronics, Computer and Electrical Engineering for Health" (ISMTECEE-2024) Under IEEE student branch (Code:12901) from 29th -1st, Feb **2024** as Program Chair.
3) Organized 2 days 4th National Conference on Recent Trends in IoT, Machine Learning, Artificial Intelligence & It's application (NCRIMA **2023**) from 24th -25th, April **2023** at Department of EC, SIRT Bhopal as Program Chair.
4) Organized 2 days International Conference on Recent Trends in IoT, Machine Learning, Artificial Intelligence & It's application (ICRIMA **2022**) from 13th -14th, May **2022** at Department of EC, SIRT Bhopal as Conference Co-Chair.

Short Term Courses/ Summer/Winter/ FDP/Seminars

1) Organized 1-week Winter Course on "**VLSI Design with IoT Application**" as program coordinator and trainer at SIRT, The Sage Group from 4th –8th March **2024**.
2) Organized 2-week Winter Course on "**VLSI Design & Application of Machine Learning** as coordinator and trainer at SIRT, The Sage Group from 13th Feb to 24th Feb **2023**.

3) Organized 2-week Summer Course on "Short **Term Course on VLSI Design & Image Processing -21 (STCVDIP-21)**" as coordinator and trainer at SIRT, The Sage Group from 24th May to 4th June **2021**
4) Organized 6 Day Entrepreneurship Skill Development Programme Under Entrepreneurship Development Cell (EDC), The SAGE Group, 17th - 22nd, May **2021** as Convener.
5) Organized **1-week Short Term Course on VLSI Design** in **2020** at SIRT Bhopal.
6) Organized one week **AICTE Sponsored STTP** on "POST COVID Challenges in Teaching & Learning" as Co-coordinator in department of EC, SIRT Bhopal from 14th -19th, Sept **2020**.
7) Coordinate one-day Entrepreneur Awareness Drive (EAD) with E-cell, **IIT Kharagpur** at SIRT, BHOPAL, on 16th Oct **2019**.

Delivered Expert Talks

1) Delivered an Expert Session on "**Innovation to Impact: Turning Ideas into Sustainable Venture**s" on **01-01-2026** held at **Oriental College of Technology, Bhopal**.
2) An Expert Session Delivered at Govt. ITI Govindpura, Bhopal on **Solar Entrepreneurship** in Entrepreneurship Skill Development Program (ESDP) by NIESBUD, initiated by the Ministry of Skill Development and Entrepreneurship, GoI & Ministry of New & Renewable Energy (MNRE) on 14 Nov 2025.
3) Expert in one session of Cadence Virtuoso EDA tool in STCVD 2014 at **MANIT Bhopal.**
4) Delivered an Expert talk on Technology & Innovation in **Entrepreneurship Start-up Basics & Idea Validation** at SIRT-E, Bhopal 10th March 2025.
5) Delivered an Expert talk on **Entrepreneurship and MSME Incubation Centre** in National Start-up Day and Youth Day at Sage University Bhopal on 22nd Jan 2025.
6) Delivered an Expert talk on **Entrepreneurship and innovation,** at SISTECH Gandhinagar, Bhopal on 30th Nov 2024
7) Delivered an expert talk on "**Roadmap for patent filing in India**", in FDP on Importance of IPR and Innovations in the Industries and Academics at **Parul University Vadodara, Gujarat on 7 April 2023.**
8) Invited as Speaker in ambitious science & technology event "**Madhya Pradesh Vigyan Sammelan and Expo (MPVS-2021) at IIT Indore at 24 dec2021**, which is in collaboration with Vijnana Bharati, Malwa Prant and MPCST, Govt of MP. The theme for event is chosen as "Collaborative Ecosystem of Traditional & Modern Science for Viksit Pradesh - Aatmanirbhar Desh". Conclave entitled as "**Fabless and Fab Semiconductor Ecosystem**".
9) Delivered an Expert talk on **Performance Parameters of Digital Portable Devices,** at Dept. of EC, **Bansal Group of Institutions**, Mandideep on 29th June **2021**.
10) Delivered an Expert talk on **IPR basics and Patent Filing in India** at Dept. of EC, **Sage University Indore** on 10th June **2021**.

11) Delivered an Expert talk on **Patent Filing Procedure in India** at **Sage University Bhopal** on 31st Jan **2021**.

Fellowships Received

1) Received Gate Fellowship in **2007**
2) Received full fellowship for attending 23rd Int. Symposium on VLSI Design and Test (VDAT-2019) at 3rd -5th July **2019**, at **IIT Indore**.

Awards

1) Sage Chairman Award in **2020** & **5** Atma-manthan award in May **2025**, August **2023,** July **2020**, July **2019** and May **2016**.

2) **Most Popular Faculty** award in the Sage annual award Ceremony at 22 May 2025. SIRT Bhopal

3) **Advisor** in National Student Conference 2025 organised by Sage Group of Institutions Bhopal on 5th April 2025

4) Received Reviewer Certificate by SCI indexed Journal "**Analog Integrated Circuits and Signal Processing**" Springer for reviewing 9 papers in 2025.

5) Received a Reviewer Certificate from the World Conference on Computational Science and Technology (WcCST 2026), Conference Record Number #67302, which was technically co-sponsored by IEEE CIS held on 26th – 27th, March 2026 at Chandigarh University Punjab, India.

6) Received Reviewer Certificate by International Conference on Next Generation Technologies for Sustainable Development (ICNGT-2025), organized by SVKM's NMIMS, Shirpur Campus on March 28 - 29, 2025.

7) Received **Certificate of Appreciation** as Reviewer in IEEE 6th Parul University Int. Conf. on Engineering & Technology PiCET 2024, organized **by Parul University, Vadodara,** held at 3-4, May 2024.

8) As a Mentor **won** first Prize in Smart India Hackathon **2022** (In Hardware edition) with title SIRT Agritech in Aug 2022 Kottayam Kerala, India.

9) Attended Board of Studies (**BoS**) Meeting for refining the Syllabus & Scheme of BSc. (CS) at IEHE Bhopal on 10-06-2022.

10) Attended Board of Studies (**BoS**) Meeting for refining the Syllabus & Scheme of B.Tech & M.Tech at RNTU Bhopal on 11-06-2022.

11) 3 of my paper are accepted for Indexing at **RSquareL with value 77, 81, 83 through Global Academician Research Network**. PAPER ID (i) V1I3293, (ii) V1I3294, (iii) V1I3295.

12) Received appreciation as Reviewer from SCI "**Journal of The Institution of Engineers (India): Series B' Springer**" on 18th Sept 2020.

13) Received **Certificate of Appreciation** as Reviewer in 3rd Int. Conf. PiCET 2020, on **SMART ENGINEERING** jointly organized **by Parul University, Vadodara, India & University of Mons (UMONS), Belgium**, held at 6th – 7th Nov 2020.

14) Appointed as a Proctor Coordinator, in an Online FDP on 'Demystifying 5G RF ASICs', scheduled during 24 Aug 2020 to 4 Sept 2020, conducted by NIT PATNA and Electronics and ICT Academy (An initiative of the Ministry of Electronics and Information Technology (MeitY), Govt. of India).

15) Invited as "**Chief Guest**", in the National webinar entitled, "**New Paradigm of Industry Research Trends in VLSI and Data Science**" on 2nd Aug, 2020 organized by Bharat Institute of Engineering and Technology, Hyderabad, Telangana in association with ISTE, and IIC MHRD.

16) Got **SRIJAN 2018 Award**.

17) Participating as a Mentor in HACKATHON-2017 at COEP, Pune under the Ministry of MIETY, make an Android App for Kids education named "WeSMART" on 1-2 April 2017

18) Worked as an IIM Test Centre Administrator Procter at SVCE Indore by PROMETRIC in 2010.

19) Seminar on "Soft Handoff in CDMA" at I.E.T. DAVV INDORE in 2008.

20) Qualified in GATE-EC **2007.**

21) Written qualified of Graduate33 Engineer Trainee in **ECIL, Ref No: 6376 in 2007**.

Organized Webinar/ Expert talks under EDC

1. Organized One Day Awareness programme (EAP) with Center for Entrepreneurship Development MP (CEDMAP) Bhopal under office of the development commissioner, Ministry of Micro, Small & Medium Enterprises(MSME), Govt. of India on 6th Jan 2023.

2. Organized an International Webinar under EDC Cell on the topic of "Internationalisation of SMEs and market orientation" on Saturday 26th Sept 2020 by Dr Soniya Billore Department of Marketing School of Business and Economics Linnaeus University, Vaxjo, Sweden.

3. Coordinate 6th India International Science Festival (IISF)-2020 on "The Energy Centre 2020- Renewable Energy for Self Reliance & Global Welfare by Vijanana Bharti (Vibha) at SIRT Bhopal under EDC cell on 16th Dec 2020.

4. Coordinate an Event on Atmanirbhar Bharat, by India Cowin Action Network (I-CAN's)- Y4AB (Yuva for Atmanirbhar Bharat) at 15th Oct 2020 at 6:00- 7:00 PM , at facebook.com/INDIACAN2020/

i. Summary: In the Gracious Presence of Padmashri Kailash Kher (Spiritual Singer & Music Composer), Dr. Vinay Sahasrabuddhe MP Rajya Sabha , Chairman ICCR, Shri Om Prakash Sakhlecha, Minister of Science & Technology, MSME Govt. of MP.

5. Organized an International Webinar under EDC Cell on the topic of "Internationalisation of SMEs and market orientation" on Saturday 26th Sept 2020 by Dr Soniya Billore Department of Marketing School of Business and Economics Linnaeus University, Vaxjo, Sweden. More than 290+ participation from all over the India.

6. Organized "3 day National Webinar on Incredible Journey of Entrepreneurs" Under Entrepreneurship Development Cell (EDC) SIRT, the Sage Group, from 29th - 31st August, 2020. Speakers from various Startups founders & IIT alumnus. Got Participation Across all over the India mostly from MP, Rajasthan, Gujarat, West Bengal, Jharkhand, Bihar, UP etc. Total participation was 500+.

7. **Tips For Gate Examination** by **Er. Ankit Rathore** (Ass. Manager IOCL & **Gate Air 70**) On 24th March 2020.

8. **Live Your Passion And Ride Your Attitude** by **Er. Anupam Singh Parihar,** Founder of DOCHAKI, CUSTOM MOTOR BYKE DESIGN PUNE, BHOPAL on 30th April 2020.

9. **Identification Of Neurological Disorders Using Eeg Signals** by Dr VARUN BAJAN (FACULTY IIITDM JABALPUR) on 01st May 2020.

10. Coordinate one day Entrepreneurship expert session titled as "ENVISAGE" under EDC SIRT, on 15th Feb 2020.

11. Coordinate one day Entrepreneurship expert session titled as "ENVISAGE" under EDC SIRT, on 24th Feb 2020.

12. Organized an expert session on "Achieving Problem- Solution Fit & Product-Market Fit" by Dr. P Prashant, IIC President, NISP Coordinator, Deputy Dean(I&A), AP, Khalsa College of Engineering & Technology, Amritsar Punjab on 29th Jan 2022 under IIC SIRT in association with EDC The Sage Group.

13. Organized one webinar on "Session on Building an Innovation/Product Fit to Market" by Er. Anupam Singh Parihar, Founder of Dochaki, Bhopal & Pune,on 8th june 2021, under Institute Innovation Council (IIC) SIRT, in association with Entrepreneurship Development Cell (EDC) Sagar Group of Institutions, The SAGE Group.

14. Under planning for **Center of Excellence** in the department of Electronics & Communication Engineering SIRT, organized lecture series on **Robotics** in the association **with IISER Bhopal,** under the **PMRF scheme,** by **Er. Manav Mishra,** Ph.D. student, EECS department Indian Institute of Science Education Research, Bhopal from 29th Jan 22 to 25th Feb 22.

Mtech Guided

Sr.	Brach	Roll No.	MTech Scholar Name	Date of Viva	Title of Thesis
SESSION 2016-17					
1	VLSI	0133EC13MT21	Vandana Prajapati	25-11-2016	Implementation and Power Analysis of Toggle Clock Gated ALU
SESSION 2017-18					
2	VLSI	0133EC13MT34	Nidhi Sharma	17-02-2018	Design and optimization of Fin-FET based SRAM cell in NANO Scale Technology
3	VLSI	0133EC13MT27	Ankit Upadhyay	01-05-2018	High performance VLSI architecture for transpose form filter using integrated module
SESSION 2018-19					
4	EC	0133EC13MT06	Harsha Dharmik	20-07-2018	Design implementation & FFT analysis of clock generators using DPLL based on C5 SCMOS
5	VLSI	0133EC13MT35	Md. Farid Khan	18-08-2018	A Novel Technique in Adiabatic Logic for Ultra Low Power in DSM Technology
6	VLSI	0133EC13MT25	Abhijeet Kumar Singh	18-08-2018	A Novel Technique to Improve Performance evaluation of Domino Logic Circuits in CMOS and Fin-FET Technology
7	VLSI	0133EC16MT20	Pratibha Gour	09-11-2018	IDFS : An algorithm for reducing worst leakage power in Fin-FET VLSI Circuits
8	VLSI	0133EC13MT42	Sneha Meshram	29-12-2018	CMOS Based Low Power Voltage Reference Generator Is Optimized In 32nm Technology
9	VLSI	0133EC13MT36	Nitin Mishra	14-04-2019	Designing of Model Predictive Controller for LED Flood FPGA
SESSION 2019-20					
10	VLSI	0133EC14MT40	Veena Yadav	28.12.2019	A Verilog Implementation of Built in Self-Test with Linear Feedback Shift Register for Performance Improvement

11	VLSI	0133EC17MT24	Mr. Harshmani Yadav	28.12.2019	Design of Digital Circuit for Improved Voltage Using GDI Technique
SESSION 2020-21					
12	VLSI	0133EC15MT29	Anjali Patware	06.02.2021	Dynamic Power Reduction By CNTFET Based Adiabatic Logic Circuits At UDSM Technology
13	VLSI	0133EC18MT41	Shiju Koshy	17.03.2021	RF Receiver Circuit Designing using Sample and Hold Technique
14	VLSI	0133EC17MT20	Amir Siddiqui	17.03.2021	Design and Performance Improvement of 64-Bit Rounding Based Approximate Multiplier for High Speed FPGA
15	VLSI	0133EC15MT36	Namrata Sharma	15.04.2021	Low Power High Speed Domino Circuit Design Using CNTFET
16	VLSI	0133EC15MT41	Smitha Raj Acharya	15.04.2021	Development and Design for Optimization of Low Power Level Shifter using CNT technology
SESSION 2021-22					
17	EC	0133EC17MT18	Udita Pathak	18.09.2021	Dust Identification And Removal For Digital Single Lens Reflex Camera Using Morphological Operation
18	EC	0133EC18MT13	Khushbu Pathak	18.09.2021	Design And Analysis Of Microstrip Patch Antenna Array For 5G Communication Applications
19	VLSI	0133EC18MT34	Parul Sharma	29.03.2022	Design and Analysis of Low Power High-Speed Ternary Full Adder
SESSION 2022-23					
20	EC	0133EC17MT05	Asim Ali Khan	05.08.2022	A Multi SVM Machine Learning method for Drowsiness Detection using EEG signal
21	EC	0133EC15MT08	Kalyani Tomar	08.08.2022	A Novel Approach For Melanoma Skin Cancer Detection Using Dermoscopy Image Processing
22	EC	0133EC18MT01	Abhishek Kumar Sinha	23.09.2022	Koch Fractal Curve based Fractal Antennas for Multiband Applications
23	EC	0133EC18MT09	Chitralekha Nagle	30.12.2022	Expectation Maximization Clustering Using Gaussian Mixture Models For Energy Efficient Routing Protocol In Wireless Sensor Network

24	VLSI	0133EC17MT29	Pooja Shakya	14.02.2023	Implementation Of DHT Algorithm for VLSI Architecture
SESSION 2023-24					
25	VLSI	0133EC19MT29	Diksha Patel	14.07.2023	Medical Image Fusion based on Non-subsampled Contourlet Transform
26	VLSI	0133EC21MT09	Amit Sahani	06-05-2024	Design & Verification Of SPI Protocol With 2D Memory Using HDL Language Verilog And Universal Verification Methodology
SESSION 2024-25					
27	VLSI	0133EC19MT37	Rishabh Singh	25-07-2024	Low Power Nano-Scale Based Adiabatic Logic Circuit Design In ULSI Applications

BE Undergraduate Major Project guided

1) Sharmin Sami, Rani Patel Sweety Kumari , and Monika Chouhan (2015-16)
   Title: **KEYPAD INTERFACING USING FPGA KIT**

2) Areeb Ahmad, Deenanath Prajapati, Deepak Shah, Deepanshu Gupta (2015-16)
   Title: Arduino Based Silicon Eye Using Ultrasonic Sensor for Blind Person

3) Akash Sharma, Divya Maheshwari, Aakash Shewani, Shashi Singh and Dushyant
   Title: **Dimension Detection by Surveillance Robot** (2016-17)

4) Shrutika Mahalle, Vibha Saroj, Shruti Soni, Shiwani Agrawal, and Shivam Agrawal (2016-17)
   Title: **Flex Sensor Based Robotic ARM using Microcontroller**

5) Ravi Ranjan Kumar, Rakesh Kumar, Shitanshu Shekhar, Shweta Singh, Shalini Shrivastava (2017-18) Title: **Child Traking Device**
6) Medha Rawat, Ragini , Roshni Pawar, Sidhdhant (2017-18)
   Title: **Motion Estimation Using Optical Flow in MATLAB**

7) Arunima, Amit Agrawal, Anchal Dubey (2018-2019)
   Title: Smart Dustbin: **Waste Separate and Garbage Monitoring**.

8) Anukul Sahu, Abhishek Patel, Himanshu Chopde (2022-23)
   Title: **Raspberry Pi Based Vehicle starter on face Detection.**

Workshop /Webinar/FDP Attended

1) VLSI Design (26-28 June, 2013) at MANIT, Bhopal
2) VLSI Design (26-28 Dec, 2013) at MANIT, Bhopal
3) Ultra Low Power RISC Microcontrollers & its Applications on Feb 15-16, 2014 at MANIT, Bhopal
4) Next Generation Education Campus for Connected Learning, January 17th 2014, MANIT, Bhopal

5) Nanotechnology Journey from Quantum Physics to Nano engineering, April 2nd 2014 at IIT ROORKEE
6) Custom Designer tool by Synopsys from May 28th -30th, 2014 at C-DAC NOIDA given by SYNOPSYS Experts.
7) Engineering Education and Research Seminar, November 5th 2015 by National Instrument India at Courtyard Marriott Bhopal
8) Hands-on Training on Electronic Devices Automation, 5th – 6th April 2016, MANIT Bhopal
9) Research Why How and When, by ACM Chapter Bhopal, 15th April 2017
10) Emerging Nano-Electronics Devices Modeling, Simulation and Application, June 26th – 30th, 2017 at IIITDM Jabalpur under AICTE (QIP).
11) FDP on MATLAB & It's Application in Computational Intelligence, Dec 14th -19th, 2017 at MANIT BHOPAL organized by Electronics &ICT and IIITDM JABALPUR.
12) FDP on English Communication, Dec 26th -39th, 2017 at SIRTS Bhopal.
13) Attended 23rd Int. Symposium on VLSI Design and Test (VDAT-2019) at 3rd -5th July 2019, at IIT Indore.
14) 3-days "Faculty Development Program for Student Induction (FDP-SI)" during 16 - 18 July, 2019 at Sagar Institute of Research Technology, Bhopal organized by All India Council for Technical Education(AICTE).
15) 1 WEEK "FDP" during 11th – 16th, May 2020, conducted by TPIIC, Sage University, Indore.
16) Online STTP on Python 3.4.3 during 29th May – 2nd June 2020, Conducted by Dr. K.N Modi University Association with Spoken Tutorial-IIT Bombay, funded by the National Mission on Education through ICT, MHRD, Govt. of India.
17) 1 WEEK "FDP cum Workshop" on "Research Methodology with Hand on Research Paper Writing", during 1st – 5th, June 2020, conducted by EC Dept, Sage University, Indore.
18) 1 week Online FDP on Research in Modern Era during 1st – 5th June 2020 conducted by J. C. Boss University of Science & Technology, YMCA, Faridabad.
19) 3 days' workshop on The Growing Role of IoT in Covid 19 & Health Care, by Shriram K. Vasudevan from 8th – 10th June 2020, organized by Rajiv Gandhi Proudyogiki Vishwavidyalaya, Bhopal with Department of Information Technology, Shri G. S. Institute of Technology & Science, Indore (M.P.) in association with WILEY India Pvt. Ltd.
20) 5 days FDP on "Recent Trends in VLSI Design" from 22nd – 26th June 2020, organized by Dept of EC, LNCTS Bhopal
21) 3 days' FDP/ Sage Summer School on "ICT Enabled Teaching Learning" from 23rd – 25th June 2020, organized by Dept. of EC, SIRT Bhopal association with Wiley, IEEE MP Sub Section.
22) 3 days' FDP "HANDS-ON EXPERIENCE WITH ARDUINO USING VIRTUAL TOOL" from 25th – 27th June 2020, organized by Dept. of EC, PSCMR in association with IEEE student chapter & IIC – MHRD.
23) 1 days' Workshop/ Sage Summer School on "Intellectual Property Rights" on 10th July, 2020 organized by Dept. of EC, SIRT Bhopal association with MPCST.
24) Three Day International Webinar On "Research Applications in Artificial Intelligence, Data Science and Emerging Technologies" 17 to 19th July, 2020 Organized by Department of Electronics and Communication Engineering, Bharat Institute of Engineering and Technology, Hyderabad, Telangana.
25) AICTE Sponsored Short Term Training Program (STTP) On "Embedded System Design with IoT", Organized by Department of ECE, SIRT, Bhopal from 27 July to 1 Aug 2020.

26) One Week Online International Faculty Development Programme (IFDP) on "Innovative and Entrepreneurial Ecosystem in Engineering for Post COVID-19 Pandemic" Under Institution's Innovation Council, SIRT (MHRD), organized by Department of ME, SIRT, Bhopal from 27th – 31st July, 2020.
27) AICTE Sponsored Short Term Training Program (STTP) On "Raspberry Pi & Python Programming", Organized by Department of ECE, SIRT, Bhopal from 24-29 Aug 2020.
28) AICTE Sponsored One Week Online Short-Term Training Program on "Electric Vehicles: Challenges and Opportunities", Organized by Department of EX, SIRT, Bhopal from 24 - 29 Aug 2020.
29) Two day national FDP on "Research Project Grant and Patent Filing" on 19-20th October, 2020, Organized by Department of Electronics and Communication Engineering, Bharat Institute of Engineering and Technology, Hyderabad, Telangana.
30) One week AICTE Training and Learning (ATAL) Academy Online FDP on "Internet of Things (IoT)" from 2020-10-13 to 2020-10-17 at Institute of Engineering and Technology Devi Ahilya University Indore.
31) AICTE Sponsored Short Term Training Program (STTP) On "Computational Technique", Organized by Department of ECE, SIRT, Bhopal from 2nd -7th Nov 2020.
32) International FDP on 'New Paradigm of Next Generation Electronics and the Future trends in Electronic Systems' on 19th Jan-21th Jan 2021, Organized by Department of Electronics and Communication Engineering, Bharat Institute of Engineering and Technology, Hyderabad, Telangana.
33) Successfully completed 1 AICTE Training and Learning (ATAL) Academy Sponsored Online FDP on Emotional Quotient Intelligent quotient and Social quotient, 18th to 22nd Oct. 2021 conducted by SIRT Pharmacy Bhopal.
34) One week AICTE Training and Learning (ATAL) Academy Online FDP on " Advanced 3D Design and Printing for functional applications " from 25-30, Dec 2023 at OIST Bhopal.
35) 2 Days Seminar on IPR organized by Department of CSE SIRT in association with MPCST from 19th – 20th Jan 2024.
36) FDP on "Empowering Research & Innovation through IPR, ICT and RM for academic Excellence" at SIRTE Bhopal from 17 -21 February 2025.
37) One-week STTP on "**Augmented Reality in Education**" at **NITTTR Bhopal** from **17th to 21st November 2025**. The program enhanced his understanding of AR tools, immersive learning design, and technology-enabled pedagogy. He actively participated in hands-on sessions and collaborative activities, gaining valuable insights for academic innovation.
38) One-week STTP on "**Aero sustain: Drone for Sustainable Future**" at Department of EC, MPSTME NMIMS Deemed to be University Mumbai from **15th - 19th Dec 2025**. Key objective of this FDP is to equip faculty and researchers with comprehensive knowledge and practical skills in drone technology and its application in solving real-world sustainability challenges.

Webinar / Talks attended during Lockdown:

1) IEEE Remote Access: Strategies and Tips to Enhance Learning, on 7th May 2020, conducted by SIRT Bhopal association with IEEE.
2) International SAGE TALK on Recent Advances in Cloud & Edge Computing and the Aneka 5G Cloud Platform by Prof Rajkumar Buyya, Director, CLOUDS Lab, University of Melbourne, CEO, Manjrasoft, Australia, organized by Department of Computer Science and

Engineering, Sagar Institute of Research & Technology, Bhopal association with ACM-W, CSI, IEEE-MP.

3) India First Leadership Talk webinar with Prof D. P. Singh, Chairman UGC Broadcasted on 9th May, 2020 by MHRD's Innovation Cell.
4) Online Quiz on "COVID-19 Awareness Programme" for commitment to discharge the service to the nation, on 12th May 2020, conducted by Gandhi Institute of Excellent Technocrats, Ghangapatna, Bhubaneswar.
5) Leadership Talk with Dr. Pramod Chaudhari, Founder, Chairman, Praj Industries Limited and Dr. Abhay Jere, Chief Innovation Officer MHRD Innovation Cell, Saturday, 16th May 2020 at 01.00 PM by MHRD's Innovation Cell.
6) India's First Leadership Talk Series Session with Mr Mahesh Babu CEO Mahindra Electric Mobility Ltd Saturday, 23th May 2020 at 01.00 PM by MHRD's Innovation Cell.
7) Dr. Abhay Jere (Chief Innovation Officer- MHRD Innovation Cell, Govt. of India) Hosting Live session of Leadership Talk with Dr. Nilesh N Oak, Expert (Indian Civilization & History), Saturday, 30th May 2020 at 01.00 PM by MHRD's Innovation Cell.
8) Leadership talk with Ms. Ashwini Deshpande (Co-Founder & Director Elephant Design) held on 6th Jun by MHRD's Innovation Cell.
9) Leadership Talk with Shri R Subrahmanyam, IAS (Secretary Ministry of Social Justice & Empowerment) held on 13th Jun by MHRD's Innovation Cell.
10) Leadership Talk with Shri Shridhar Venkat, CEO Akshaya Patra Foundation held on 20th Jun by MHRD's Innovation Cell.
11) Leadership Talk with Shri Dipendra Manocha, (Motivational Speaker) held on 27th Jun by MHRD's Innovation Cell.
12) Webinar on "5G Technology & IoT for Healthcare" on 27th June 2020, Organized by Dept of EC, Chouksey engineering College Bilaspur(CG) in association with IEEE sc.
13) Sage Talk on "The coming AI Revolution in Digital Forensics", on 12th June, 2020 organized under by Dept of EC, SIRT Bhopal association with Wiley Webinar Series.
14) Sage Talk on "Fine Tuning Neural Network", on 10th June, 2020 organized under by Dept of EC, SIRT Bhopal association with Wiley Webinar Series.
15) Sage Talk on "Device Design for Combating Emerging Leakage Mechanisms in the Novel Nano Scale FET Architecture", By Dr. A.K Jain, PDF from Univ. of Singapore, on 15th July 2020 organized under by Dept. of EC, SIRT Bhopal
16) Sage Talk on "Role on HAM Radio in Disaster", on 15th July, 2020 By Mr. J.S. Bhide, VP, Ameteaur Radio Society, organized under by Dept. of Applied Science, SIRT Bhopal.
17) Sage Talk on "Construction Safety Measurement", on 11th July, 2020 By Prof. Devansh Jain, AP Dept of CE, UIT RGPV, organized under by Dept. of Civil Engg, SIRT Bhopal.

Participation in Online Quiz

1) Online Quiz on "Research Publication and Patent Creation Quiz" conducted by Bharat Institute of Engineering and Technology, Hyderabad, Telangana on 6/21/2020.
2) Online Quiz on "Low Power VLSI Design Quiz" conducted by Bharat Institute of Engineering and Technology, Hyderabad, Telangana on 6/22/2020.
3) Online Quiz on "VOCAL FOR LOCAL" conducted The Self Reliance Mantra" conducted by School of Entrepreneurship Skills, Bhartiya Skill Development University Jaipur in association with Management & Entrepreneurship and Professional Skills Council (New Delhi), MSME-DI, Government of India & Global Foundation for Skill Development and Entrepreneurship.

4) "E-Quiz of Atmanirbhar Bharat -Strengthen the Future" conducted by School of Entrepreneurship Skills, Bhartiya Skill Development University, Jaipur in association with The Employers Association of Rajasthan & Global Foundation for Skill Development and Entrepreneurship.
5) Online Quiz on "COVID-19 Awareness Programme" for commitment to discharge the service to the nation, on 12th May 2020, conducted by Gandhi Institute of Excellent Technocrats, Ghangapatna, Bhubaneswar.

Publication:

- In International Journals: **Appendix A**

Reviewer: Reviewer of various SCI indexed journal like –

1) Analog Integrated Circuits and Signal Processing" Springer
2) Taylor & Francis - International Journal of Electronics,
3) John Willey & Sons- International Journal of Numerical Modeling,
4) International Journal of Computers Communication and Control,
5) Springer Journal's -Journal of The Institution of Engineers (India): Series B,
6) Journal of Nano electronics and Optoelectronics
7) In Journal of Computational Electronics –Springer
8) ICIC-2015 IEEE conference

Editorial Board:

(i) Appointed as Reviewer in the World Conference on Computational Science and Technology (WcCST 2026), Conference Record Number #67302, which was technically co-sponsored by IEEE CIS held on 26th – 27th, March 2026 at Chandigarh University Punjab, India
(ii) Invited to join the Technical Program Committee (TPC) for the International Conference on Innovation in Computing, Data, and Electronics (InCODE-2K26), organized by the Oriental Institute of Science and Technology, Bhopal, scheduled for 9–10 October 2026
(iii) Appointed as reviewer in Inter. Conference held in 2025 at NMIMS.
(iv) Appointed as **Sub-Reviewer** in Parul University International Conference on Engineering and Technology: SMART ENGINEERING 2020 PiCET2020.
(v) Appointed as **Reviewer** in 10th International Conference on Electronics, Communications and Networks (CECNet), Oct. 25-28, 2020 online at Seoul Republic of Korea.
(vi) Appointed as **Reviewer** in 2020 2nd International Conference on Computer, Communications and Mechatronics Engineering (CCME) will be held in Xiamen, China during December 20-21, 2020.
(vii) Journal of Electrical and Electronics Engineering (JEEE**)**, Science PG Group since 16th April 2019.
(viii) Join Micro and Nano-systems journal as a "Bentham Science Ambassador" from your country "India**.**

Personality Traits	Sincere, Co-operative and Self motivated
Strength	Result oriented, Positive attitude, Sincerity, Ability & willingness to learn

Personal Information:

- **Date of Birth :** 17-12-1983
- **Father's Name :** Mr. M.S. Panwar
- **Category :** General
- **Marital status :** Married
- **Nationality :** Indian

- **Hobbies** **:** Reading books, surfing and visiting
- **Address** **:** 140, Aradhana Nagar, Bhopal (M.P.)

Declaration:

I hereby declare that the above stated facts are true and complete to the best of my knowledge and belief.

DATE: 02/04/2026

PLACE: BHOPAL

(Dr. UDAY PANWAR)